WE CLAIM:

1. A system for enabling device communication in an expanded computing device comprising:

a first integrated chip having a first register and a second register therein;

a second integrated chip having a third register and a fourth register therein;

a first serial link coupled between the first register and the third register; and

a second serial link coupled between the second register and the fourth register.

2. The system of claim 1 wherein the first integrated chip is an application specific integrated chip.

3. The system of claim 2 wherein the first integrated chip is configured to enable the transfer of data to the second integrated chip without using cashing.

4. The system of claim 2 wherein the second integrated chip is configured to enable the transfer of data to the first integrated chip without using cashing.

5. The system of claim 1 further comprising a primary bus coupled to the first integrated chip.

6. The system of claim 1 further comprising a secondary bus coupled to the second integrated chip.

7. The system of claim 5 further comprising a first interface coupled between the primary bus and the first register and the second register.

8. The system of claim 6 further comprising a second interface coupled between the secondary bus and the third register and the fourth register.

9. A method of transferring data between a first device having a first integrated chip therein and a second device having a second integrated chip therein, to enable an expanded computer system, the method comprising:

receiving a first data at the first integrated chip; and

independently writing the first data to the second integrated chip.

10. The method of claim 9 wherein the act of independently writing is performed by the first integrated chip.

11. The method of claim 10 wherein the act of independently writing writes the first data independently of an operating system.

12. The method of claim 10 wherein the act of independently writing writes the first data independently of hardware.

13. The method of claim 9 wherein the act of independently writing defines a transparent transaction.

14. The method of claim 9 wherein the act of independently writing is performed across a serial connection.

15. The method of claim 9 wherein the second integrated chip is enabled to independently write a second data to the first integrated chip.

16. The method of claim 15 wherein the first integrated chip writes to the second integrated chip via a serial connection.

17. The method of claim 15 wherein the second integrated chip writes to the first integrated chip via a serial connection.

18. The method of claim 17 wherein the first integrated chip and the second integrated chip operate as mirrors.

19. The method of claim 9 wherein the act of independently writing mirrors information contained in the first register to the second register.

20. A system of transferring data between two devices, comprising:

a first integrated circuit having a first register, the first integrated circuit configured to transparently transfer data to a second integrated circuit;

the second integrated circuit having a second register, the second integrated circuit configured to transparently transfer data to the first integrated circuit; and

a serial link coupling the first integrated circuit and the second integrated circuit.

21. The system of claim 19 further comprising a primary bus coupled to the first register and a secondary bus coupled to the second register.

22. The system of claim 19 wherein the first register is a PCI Standard register.

23. The system of claim 19 wherein the first register contains a base register and a limit register to indicate predetermined addresses for devices that can be found connected to a secondary bus.